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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/667,256 | 09/19/2003 | Dirk Fuhrmann | W&B-INF-1910 | 1145 |

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LERNER GREENBERG STEMER LLP
P O BOX 2480
HOLLYWOOD, FL 33022-2480

| EXAMINER | |
|---|---|
| KERVEROS, JAMES C | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2138 | |

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/667,256 | FUHRMANN ET AL. | |
| | Examiner | Art Unit | |
| | JAMES C. KERVEROS | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *19 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

This is a non-Final Office Action in response to the present US Application, filed 09/19/2003. Claims 1-11 are presently under examination and still pending in the Application.

### *Priority*

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d), for GERMAN Application No. 102 43 471.9, filed 09/19/2002. The certified copy has been filed in parent Application No. 10/667,256, filed on 09/19/2003.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 8 and 11 recite the phrase "representing", which renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. The phrase "representing" fails to clearly define the voltage signal with respect to the plurality of assessment data.

Claims 1 and 8 recite the limitation "functioning as a coded test datum", which renders the claim indefinite because the claims include elements not actually disclosed

(those encompassed by "as a"), thereby rendering the scope of the claims unascertainable.

Claims 3 and 8 recite phrase "so that", which renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention.

Claims 6 and 9 recite phrase "a voltage signal which can assume a plurality of signal levels", which renders the claim indefinite because the phrase "can assume" fails to positively define that the voltage signal has a plurality of signal levels.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 4, 5, 8, 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Huse (US Patent NO: 7,017,089) Filed: November 1, 2001.

Regarding independent Claim 1, Huse discloses an integrated memory circuit, CAM DUT (100, Figure 1) also (CAM DUT 1050, Figure 10), comprising:

A memory cell array (CAM array 110);

A test circuit (e.g., match flag) coupled to the memory cell array (CAM array 110), the test circuit (e.g., match flag circuit) generates an assessment datum (match results 115) as a result of a comparison between the values stored in the comparand register 150 and the data stored in the CAM array 110 in response to control signals from the instruction decoder 120. The CAM array 110 compares the search key against its entries and provides the match results on match lines 115 to priority encoder 160.

A coding unit (comprising a priority encoder 160 and a compare logic 165) coupled to the test circuit (e.g., match flag circuit) for coding the match results on match lines 115 to form a coded test signal (signal TFLAG). The compare logic 165 performs a comparison between an index output from the priority encoder 160 and a counter value output from the address counter 140, and generates the signal TFLAG whose logic state indicates the comparison result, described with respect to Figure 1. The signal TFLAG is a voltage signal as a function of the (match results 115).

Regarding Claims 4, 5, an external terminal on DUT 1050 for providing the test result flag TFLAG to the tester 1010, which 1010 is coupled to the DUT 1050 via a plurality of signal lines that transmit between the two entities instructions of the IBUS, data of the DBUS, compare (e.g., the index from priority encoder 160) or other results over the RBUS, and the test result flag TFLAG over another signal line. CAM device 100 is also shown as an asynchronous device. In alternative embodiments, one or more clock signals may be provided to CAM device 100 and one or more of its circuit components to synchronize operations in the device.

Regarding independent Claim 8, 10, Huse discloses a test system 1000 and a method for testing a CAM device under test, Figure 10, comprising:

An integrated memory circuit, CAM DUT (100, Figure 1) also (CAM DUT 1050, Figure 10), the integrated memory circuit containing:

A memory cell array (CAM array 110);

A test circuit (e.g., match flag) coupled to the memory cell array (CAM array 110), the test circuit (e.g., match flag circuit) generates an assessment datum (match results 115) as a result of a comparison between the values stored in the comparand register 150 and the data stored in the CAM array 110 in response to control signals from the instruction decoder 120. The CAM array 110 compares the search key against its entries and provides the match results on match lines 115 to priority encoder 160.

A coding unit (comprising a priority encoder 160 and a compare logic 165) coupled to the test circuit (e.g., match flag circuit) for coding the match results on match lines 115 to form a coded test signal (signal TFLAG). The compare logic 165 performs a comparison between an index output from the priority encoder 160 and a counter value output from the address counter 140, and generates the signal TFLAG whose logic state indicates the comparison result, described with respect to Figure 1. The signal TFLAG is a voltage signal as a function of the (match results 115).

A tester 1010 such as ATE or other test hardware and/or software that generates the instructions for the CAM DUT, coupled to the DUT 1050 via a plurality of signal lines that transmit between the two entities instructions of the IBUS, data of the DBUS, compare (e.g., the index from priority encoder 160) or other results over the

RBUS, and the test result flag TFLAG over another signal line, which corresponds to a voltage signal.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 6, 7, 9, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Huse (US Patent NO: 7,017,089) in view of Chauveau (US Patent NO: 4,864,566).

Regarding Claims 2, 3, Huse does not explicitly disclose "a digital-to-analog converter circuit", wherein the coding unit generates a plurality of voltage levels corresponding to a specific pattern of the plurality of assessment data.

In analogous art, Chauveau (US PATENT NO: 4,864,566) discloses real time analog data communication of continuous analog data, including analog encoded digital data, in a common data channel. A transmitter unit 10 includes a digital to analog converter 18, which converts digital samples stored in RAM block 16 via data lines 34 to their corresponding analog value, where transmitter 24 transmits the analog data value in the specific communication network data channel 44, Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the device of Huse by connecting the match lines 115 from the CAM array 110 to a digital to analog converter as taught by Chauveau, for the purpose of compressing the multiple lines into one output line for serial transmission to an external device. A person skilled in the art would have been motivated to employ analog encoding techniques utilized for the simple transmission of digital data through a data channel of a network-defined bandwidth. These encoding techniques improve the rate of data transfer by increasing the data representation density of the analog waveform, but without significantly increasing the required waveform bandwidth. Thus, greater rates of data can be accurately transferred within the constraining maximum bandwidth of the data channel (see, Background of the Invention).

Regarding independent Claim 6, Huse discloses a tester 1010 such as ATE or other test hardware and/or software that generates the instructions for the CAM DUT, coupled to the DUT 1050 via a plurality of signal lines that transmit between the two entities instructions of the IBUS, data of the DBUS, compare (e.g., the index from priority encoder 160) or other results over the RBUS, and the test result flag TFLAG over another signal line, which corresponds to a voltage signal.

Regarding Claims 6 and 7, Huse does not explicitly disclose a decoding circuit generating a respective pattern of assessment data in response to a voltage level, wherein the decoding circuit has an analog/digital converter circuit.

In analogous art, Chauveau (US PATENT NO: 4,864,566) discloses real time analog data communication of continuous analog data, including an analog block 76 having an

analog to digital converter 54, operating at a reference frequency f.sub.2, to receive and sequentially convert the compressed analog data segment to a corresponding digital representation for storage in a RAM block 56 as passed via data lines 68.
It would have been obvious to a person having ordinary skill in the art at the time the invention was made to deploy an analog to digital converter in the tester of Huse as taught by Chauveau, for the purpose of decompressing the received analog data segment to a corresponding digital representation for further processing.

A person skilled in the art would have been motivated to deploy an analog to digital converter coupled to a corresponding to a digital to analog converter in a communication analog channel, since analog encoding techniques are utilized for the simple transmission of digital data through a data channel of a network defined bandwidth. These encoding techniques improve the rate of data transfer by increasing the data representation density of the analog waveform, but without significantly increasing the required waveform bandwidth. Thus, greater rates of data can be accurately transferred within the constraining maximum bandwidth of the data channel (see, Background of the Invention).

Regarding Claims 9, 11, Huse does not explicitly disclose a decoding circuit generating a respective pattern of assessment data in response to a voltage level.

In analogous art, Chauveau (US PATENT NO: 4,864,566) discloses real time analog data communication of continuous analog data, including an analog block 76 having an analog to digital converter 54, operating at a reference frequency f.sub.2, to receive and sequentially convert the compressed analog data segment to a

corresponding digital representation for storage in a RAM block 56 as passed via data lines 68.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to deploy an analog to digital converter in the tester of Huse as taught by Chauveau, for the purpose of decompressing the received analog data segment to a corresponding digital representation for further processing.

A person skilled in the art would have been motivated to deploy an analog to digital converter coupled to a corresponding to a digital to analog converter in a communication analog channel, since analog encoding techniques are utilized for the simple transmission of digital data through a data channel of a network defined bandwidth. These encoding techniques improve the rate of data transfer by increasing the data representation density of the analog waveform, but without significantly increasing the required waveform bandwidth. Thus, greater rates of data can be accurately transferred within the constraining maximum bandwidth of the data channel (see, Background of the Invention).

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JAMES C KERVEROS
Examiner
Art Unit 2138

U.S. Patent and Trademark Office
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

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